



# CoreSight™ ETM-Cortex-M85 TM982

## Software Developer Errata Notice

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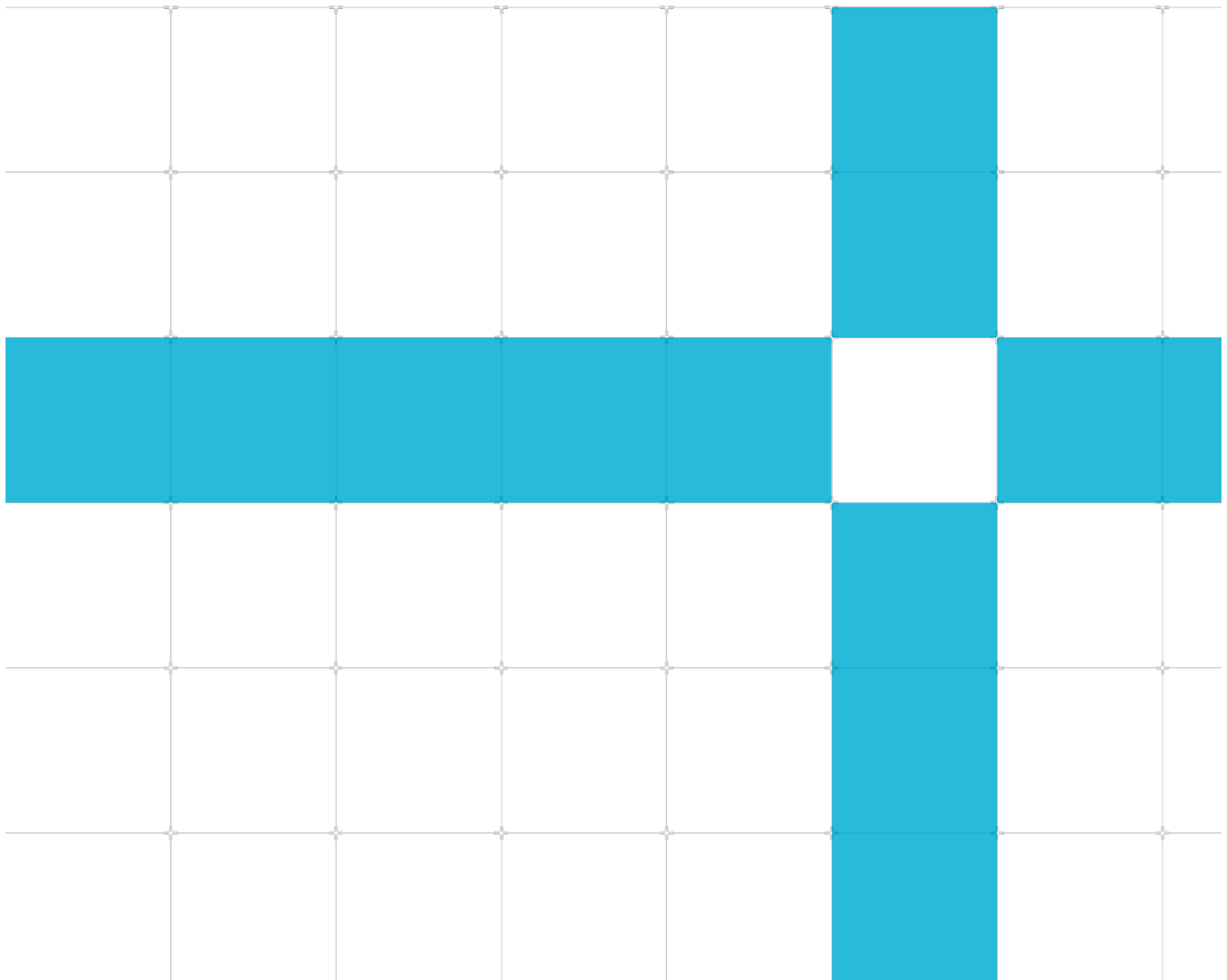
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This document contains all known errata since the r0p0 release of the product.



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# Introduction

## Scope

This document describes errata categorized by level of severity. Each description includes:

- The current status of the erratum.
- Where the implementation deviates from the specification and the conditions required for erroneous behavior to occur.
- The implications of the erratum with respect to typical applications.
- The application and limitations of a workaround where possible.

## Categorization of errata

Errata are split into three levels of severity and further qualified as common or rare:

<b>Category A</b>	A critical error. No workaround is available or workarounds are impactful. The error is likely to be common for many systems and applications.
<b>Category A (Rare)</b>	A critical error. No workaround is available or workarounds are impactful. The error is likely to be rare for most systems and applications. Rare is determined by analysis, verification and usage.
<b>Category B</b>	A significant error or a critical error with an acceptable workaround. The error is likely to be common for many systems and applications.
<b>Category B (Rare)</b>	A significant error or a critical error with an acceptable workaround. The error is likely to be rare for most systems and applications. Rare is determined by analysis, verification and usage.
<b>Category C</b>	A minor error.

# Change Control

Errata are listed in this section if they are new to the document, or marked as "updated" if there has been any change to the erratum text. Fixed errata are not shown as updated unless the erratum text has changed. The [errata summary table](#) identifies errata that have been fixed in each product revision.

## April 16, 2024: Changes in document version v5.0

No new or updated errata in this document version.

## November 23, 2022: Changes in document version v4.0

ID	Status	Area	Category	Summary
<a href="#">2755289</a>	New	Programmer	Category C	ETM can miss lockup entry when core presents WFx and lockup entry in the same cycle

## April 27, 2022: Changes in document version v3.0

No new or updated errata in this document version.

## November 29, 2021: Changes in document version v2.0

No new or updated errata in this document version.

## June 29, 2021: Changes in document version v1.0

No errata in this document version.

# Errata summary table

The errata associated with this product affect the product versions described in the following table.

ID	Area	Category	Summary	Found in versions	Fixed in version
<a href="#">2755289</a>	Programmer	Category C	ETM can miss lockup entry when core presents WFX and lockup entry in the same cycle	r0p0, r0p1, r0p2, r1p0, r1p1	Open

# Errata descriptions

## Category A

There are no errata in this category.

## Category A (rare)

There are no errata in this category.

## Category B

There are no errata in this category.

## Category B (rare)

There are no errata in this category.

## Category C

2755289

ETM can miss lockup entry when core presents WFx and lockup entry in the same cycle

### Status

Fault Type: Programmer Category C

Fault Status: Present in r0p0, r0p1, r0p2, r1p0, r1p1. Open

### Description

Due to this erratum, a lockup occurring in a rare circumstance may not be traced by *Embedded Trace Macrocell* (ETM).

### Configurations affected

This erratum affects all configurations.

### Conditions

The erratum occurs when all the following conditions are met:

- AIRCR.IESB==1
- The core is executing at negative priority
- ETM tracing is enabled

And the following sequence of events occurs in order:

1. A store operation produces a containable asynchronous BusFault
2. WFE or WFI is executed
3. A DAHB (debugger) read or write operation occurs between the WFE/WFI and the next instruction

### Implications

If the above conditions occur, an asynchronous BusFault that escalates to lockup may not be traced by ETM.

### Workaround

A workaround is not needed. This is because it is anticipated that entering a sleep mode will normally be preceded by a write to a sleep configuration register. This requires a barrier to guarantee completion and will also escalate any BusFaults that may be awaiting escalation.